A Class B Switch-Mode Assisted Linear Amplifier

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***Abstract*—A switch-mode assisted linear amplifier (SMALA) combining a linear (Class B) and a switch-mode (Class D) amplifier is presented. The usual single hysteretic controlled half-bridge current dumping stage is replaced by two parallel buck converter stages, in a parallel voltage controlled topology. These operate independently: one buck converter sources current to assist the upper Class B output device, and a complementary converter sinks current to assist the lower device. This topology lends itself to a novel control approach of a dead-band at low power levels where neither class D amplifier assists, allowing the class B amplifier to supply the load without interference, ensuring high fidelity. A 20 W implementation demonstrates 85% efficiency, with distortion below 0.08% measured across the full audio bandwidth at 15 W. The class D amplifier begins assisting at 2 W, and below this value, the distortion was below 0.03%. Complete circuitry is given, showing the simplicity of the additional class D amplifier and its corresponding control circuitry.**

***Index Terms*—Class B amplifier, class D amplifier, dead-band, distortion, half-bridge current, hysteretic controlled, parallel buck converter, SMALA, topology.**

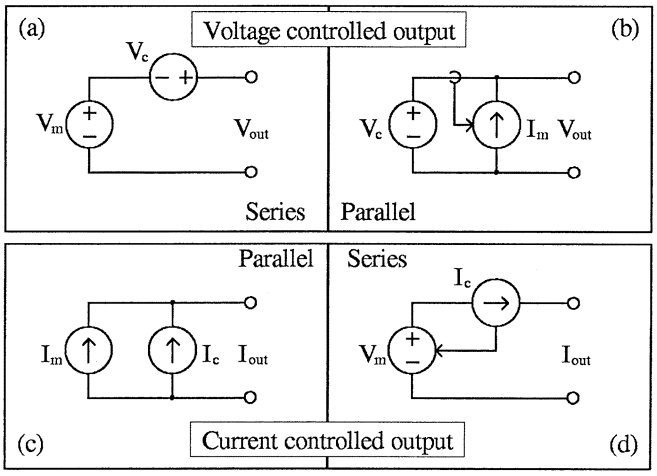

Fig. 1. Four SMALA topologies as proposed by Yundt [2]. The parallel voltage controlled output configuration (b) is preferred for audio amplifier applications.

I. Introduction

A. What Is a Switch-Mode Assisted Linear Amplifier?

A SWITCH-MODE assisted linear amplifier (SMALA) is an amplifier which is a combination of a Switchmode or Class D switching amplifier, and a linear (Class A, AB, or B) amplifier. Traditional audio amplifiers are linear amplifiers, because of their ability to deliver extremely low distortion and noise performances. However, they are heavy and dissipate a lot of power. Using switchmode techniques, class D amplifiers could potentially be very light and achieve very high efficiency. However achieving the low distortion performance required for HiFi audio has always been elusive [1].

B. Previous Related Work

A switch-mode assisted linear amplifier (SMALA) can be regarded as a relatively new topology in the field of power amplifier electronics. The idea of cascading the linear amplifier and switch-mode amplifier was discussed in 1986 by Yundt [2]. He proposed four important properties that distinguish the different composite amplifier topologies. These four properties are as follows.

1) The main amplifier may be a current or voltage output.
2) The correction amplifier may be a current or voltage output.
3) The amplifiers may be connected in series or parallel.
4) The main amplifier is controlled to the output variable or is in an impedance modifying loop.

These four properties led to four fundamental composite amplifier topologies (Fig. 1), namely series or parallel voltage controlled outputs (a, b) and series or parallel current controlled outputs (c, d). In general, Fig. 1(a) and (c) share a common philosophy, where the main (switch-mode) amplifier controls the desired output, while the smaller correction (linear) amplifier nulls errors of main amplifier. For Fig. 1(b) and (d), the correction (linear) amplifier defines the output variable, while the main (switch-mode) amplifier instantaneously reduces the effective load on the linear stage.

Audio power amplifiers require a voltage controlled low impedance output. The correction amplifier in a series cascade of two voltage sources [Fig. 1(a)] must pass the full load current, but is supplied by and delivers only a fraction of the output voltage—enough to cancel the ripple of the switchmode amplifier. In a parallel connection [Fig. 1(b)], the correction amplifier provides the full load voltage, but only a fraction of the output current under normal circumstances. However, under transient conditions, this topology can easily be designed to deliver the full load current and maintain signal fidelity.

This parallel voltage controlled topology (Fig. 2) has been further investigated in recent years [3]–[6]. An excellent mathematical examination of the tradeoffs between switching frequency, inductance value and ripple current, bandwidth and power dissipation is available [3]. It shows two key design considerations for the linear stage are obtaining a low output impedance and wide bandwidth. Finally, a number of alternative topological variations are suggested.

Three independent groups of researchers have presented experimental examples of the parallel voltage controlled topology

Manuscript received October 10, 2002; revised May 13, 2003. Recommended by Associate Editor C. K. Tse.

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Digital Object Identifier 10.1109/TPEL.2003.818825

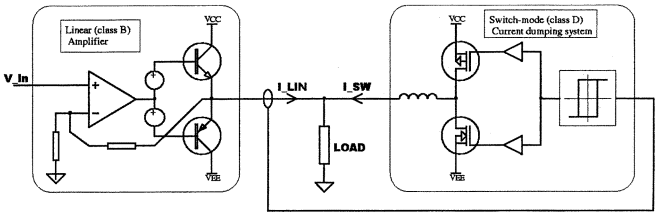

Fig. 2. Parallel voltage controlled output SMALA implementation proposed in [3].

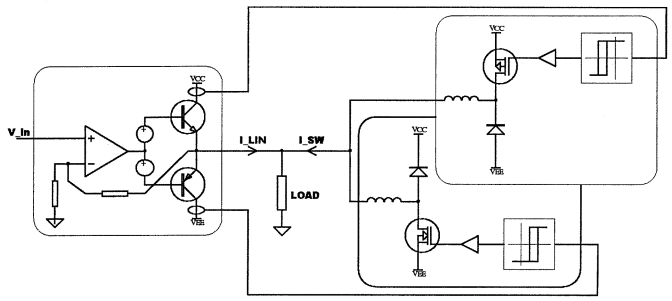

Fig. 3. SMALA implementation proposed in this paper. The novel contributions are the re-situated current sense points, and offset bias of the hysteresis controllers.

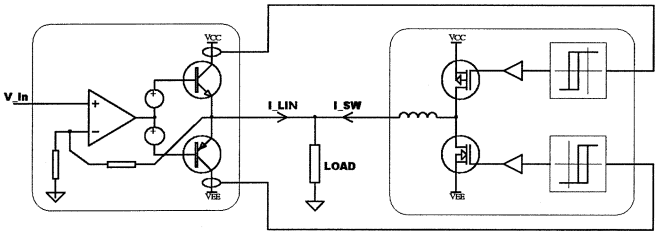

Fig. 4. Simplification of the SMALA implementation proposed in this paper (Fig. 3). This topology was not implemented because of the danger of cross conduction, and the reliance on the MOSFET body diode.

with good results [4]–[6]. Reference [4] reports an excellent result of 0.01% THD at 1 kHz from 0.5 to 50 W, and an efficiency of 90% at 50 W. A custom integrated circuit class D stage with a separate integrated circuit class B stage also achieves 0.02% THD up to 30 W with 85% efficiency at 30 W [5]. A full bridge configuration [6] achieves less than 0.1% THD at 25 W.

The technique suggested in this paper of measuring the linear amplifier output current via current shunts in the supply rails has been previously reported [5]. In that work, those two currents are re-combined to create the one controlling signal for the class D stage.

The operation with a switching deadband around zero output has also been successfully demonstrated [6], but with a complex unipolar switching full bridge stage, and two linear amplifiers for the two ends of the bridge-tied load.

C. Proposed Topology

This paper takes the parallel voltage controlled topology and suggests a novel modification of the control of the current dumping stage. The single hysteretic half-bridge current dumping stage (Fig. 2) [3] is replaced by two parallel buck converter stages (Fig. 3) as proposed in Fig. 9(d) of [3]. These operate independently: one buck converter sources current to assist the upper class B output device during the positive half cycle of the output waveform, and a complementary converter sinks current to assist the lower device during the negative half cycle.

These converters use simple hysteresis controllers servo'ed from current sense resistors placed in the supply lines of the class B output devices. In theory, this does not interfere with the stability of the class B amplifier, since the buck stages only effectively modify the load impedance seen by the class B amplifier. The linear amplifier may operate in class B, AB, or even pure class A, so long as the rising output current can be sensed in the corresponding supply rail (for the implementation presented here, in any case).

A valuable advantage of this topology and control approach is the presence of a dead-band at low power levels where neither buck converter assists. This allows the linear amplifier to supply the load without interference at low power levels, ensuring high fidelity [6].

A second valuable contribution is the simple nature of the two hysteresis controllers. Each consists of only a comparator and MOSFET driver, and requires a single low power supply rail. Complexities such as level shifting or differential amplifiers are avoided.

The two separate buck converter stages each with their own MOSFET, diode and inductor could be combined into a single half-bridge converter (Fig. 4), consisting of two MOSFET's and a single inductor. This simplification was not pursued further in this initial investigation for two reasons. First, any false turn on of one MOSFET while the other MOSFET was switching due to noise or interaction will lead to the destruction of both due to shoot-through currents. The two independent bridges is an inherently more fault tolerant design suitable for prototyping. Secondly, the body diodes of most power MOSFET's, especially higher voltage devices, have relatively poor reverse recovery characteristics, leading to higher losses, higher device stresses and potentially worse EMI, especially as switching frequencies move into the hundreds of kiloHertz. Although other alternatives exist, one of the simplest approaches to ensuring external Schottky or ultra-fast recovery diodes conduct instead of the MOSFET body diodes is to employ two independent bridges.

II. Design Considerations

A. Class B Amplifier Design

For the purpose of this investigation, a class B amplifier was preferred over class A and class AB. Class AB amplifiers are not preferred because of the step change in loop gain that occurs as the amplifier output moves from class A to B [7]. In this application, the linear amplifier generally operates below a known current set by the hysteresis thresholds of the buck controllers. This current can be set relatively low, so a class A amplifier may be a good choice in this application. However, it will always have an efficiency and power dissipation penalty compared to a class B amplifier, and since it is argued a class B can be made to have very low distortion anyway [7], a class B is chosen for this initial study.

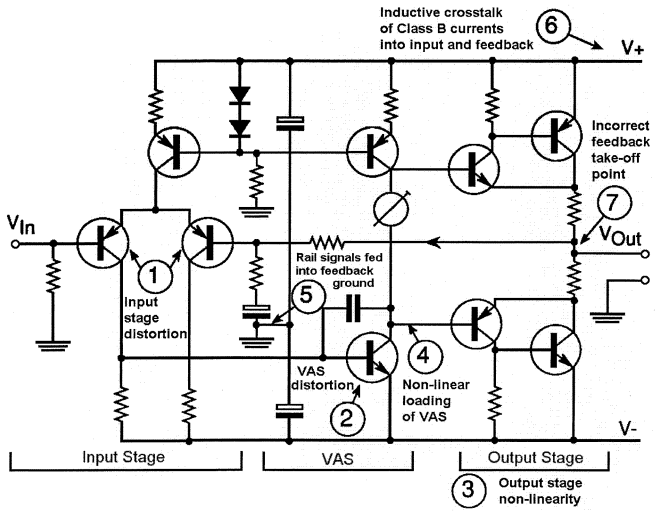

Fig. 5. Seven sources of distortion as put forward by Self [7].

In general, there are seven major distortion mechanisms in class B amplifier that when addressed lead to a good linear amplifier design [7]. These are helpfully represented graphically on the typical three stage power amplifier circuit in Fig. 5. They are discussed with specific reference to their relevance in a SMALA.

1) Input stage distortion. This is mainly caused by an unbalanced differential input pair, which leads to high frequency (HF) distortion emerging from the noise floor earlier. As frequency increases, it rises at 12 dB/octave and is mostly second harmonic. However, if the differential input pair is carefully balanced, then this distortion is typically only measurable at HF, rises at 18 dB/octave, and is almost pure third harmonic. Emitter degeneration and a current mirror on the input stage help reduce this distortion.
2) Voltage amplifying stage (VAS) distortion. Due to nonlinearity in the VAS, this distortion component remains constant until the dominant-pole frequency is reached, then rises at 6 dB/octave. The level of distortion is usually very low due to linearising local negative feedback (NFB) through the dominant-pole capacitor. Therefore increasing the local VAS open-loop gain by using a darlington for the VAS can help solve this problem.
3) Output stage distortion. In terms of a Class B amplifier, this will be a blend of large-signal, crossover, and switching distortion. The use of complimentary feedback pairs (CFPs) rather than darlington emitter followers gives better bias and thermal stability, and better linearization of the output devices all because they experience local NFB. With careful biasing, crossover distortion can be made very small. Large signal distortion caused by gain reduction of the output stage at high currents can be neglected here since once the switchmode assistance begins, the output current will remain relatively constant, at a relatively low value.

   MOSFET output stages do potentially have a higher bandwidth, however this advantage may often be lost due to the capacitive loading on the driver stages requiring more conservative compensation. They are less efficient than BJTs in a conventional linear amplifier, both because of their lower gain and their inability to approach the supply rails as closely as BJTs can. Once again, in a switchmode assisted topology, these factors are not so important.

   Distortion aside, it must be emphasised that a very low output impedance of the linear amplifier is of paramount importance in order to get a high signal-to-noise-ratio (SNR) at the output [2]. This was one deciding factor for using a BJT output stage. However, the low output impedance of a BJT output stage is dominated by the emitter resistors included for bias stability, so high loop gain in the feedback system is important. Future research needs to more carefully compare the output device justification and selection.
4) VAS loading distortion. This distortion is caused through loading of the VAS by the nonlinear input impedance of the output stage. It is normally the limiting distortion factor at low frequency (LF), typically below 2 kHz, and can simply be cured by buffering the VAS from the output stage. In a switchmode assisted amplifier, the output stage load is relatively low and output current relatively constant, so this distortion mechanism should be greatly reduced.
5) Rail decoupling distortion is a nonlinearity caused by large rail-decoupling capacitors feeding the distorted signals on the supply lines into the signal ground.
6) Induction distortion is a nonlinearity caused by induction of Class B supply current into the output, ground, or NFB lines.
7) NFB takeoff distortion is a nonlinearity resulting from taking the NFB feed from slightly the wrong place near where the power transistor Class B currents sum to form the output.

These last three distortions can all be avoided by careful PCB and power wiring layout. It was found in this work that correct placement of the decoupling capacitors and careful connection of the two sub-systems was vital to reducing distortion. The situation here is helped since the current levels in the linear amplifier are reduced, but made more difficult by the high frequency nature of the (ripple cancellation) currents flowing in the output stage.

The final linear amplifier design shown in Fig. 6 is based closely on the "blameless" example 50 W amplifier design presented by Self [7]. The only unusual feature is the inclusion of current sensing resistors in series with the output stage at each supply rail. With 60 V rated output devices, ± 20 V supply rails were chosen. This allows an output power of 20 W (18 Vp) into an 8 Ω load.

The physical layout is contained on a compact single sided PCB measuring 75 by 45 mm (Fig. 8). As already discussed, this PCB was carefully laid out to avoid the introduction of avoidable distortion or noise. Single TO-220 devices are used for the output devices, which are clamped in place on the plate chassis using fold-back spring clips and insulated using thermally conductive pad material. The small metal chassis was quite sufficient for the power dissipation of the entire amplifier.

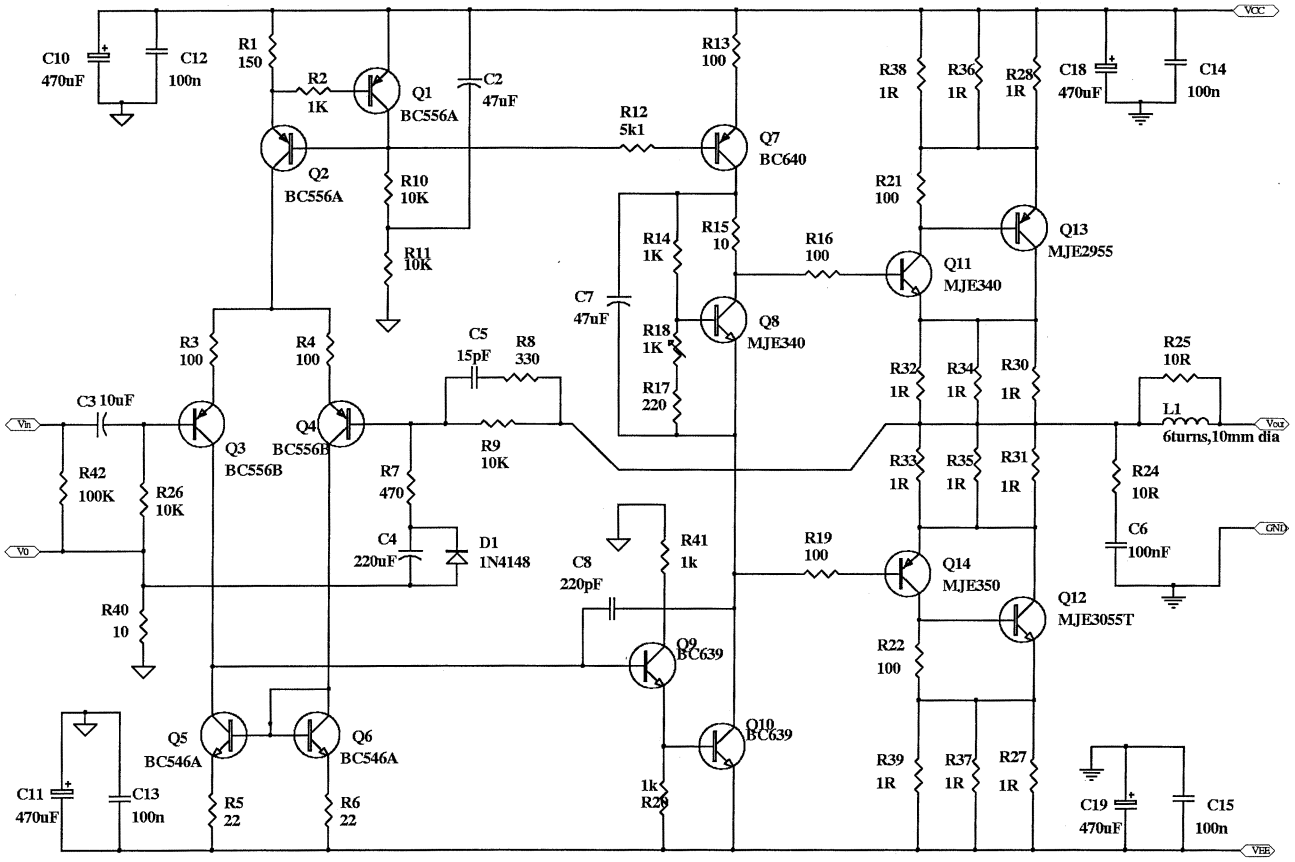

Fig. 6. Class-B amplifier circuit as implemented.

B. Class D Buck Converter Design

The Class D amplifier consists of two independent buck converters. These are controlled by the linear amplifier's output stage through the use of current sensing resistors in each supply rail. The voltage measured across these is then compared to a reference value and in turn provides hysteresis control to a MOSFET driver (Fig. 3).

The actual circuit design is very simple (Fig. 7), and the two halves are essentially identical. The heart of each circuit is the hysteresis comparator formed by a MAX941 comparator. This low power (5 mW) high speed (80 ns) device requires a 5 V supply. The TI TPS2811 MOSFET driver is also a low power (3 mA at 100 kHz, $\mathrm{CL} = 1$ nF) high speed (40 ns delay, 25 nS rise/fall) part. The use of logic level MOSFET's avoids the need for additional supply rails. The availability of logic level Pch devices is limited, and standard devices were used for testing. Because of the low current levels in this prototype, the 5 V gate drive was sufficient [8], [9].

An LM431 shunt voltage regulator is used provide a stable voltage reference for the hysteresis comparator, via a resistive voltage divider. This regulator also provides the 5 V supplies tied to the amplifier supply rails for powering the comparator and MOSFET driver. A shunt regulator allows operation with arbitrary large amplifier voltage supply rails. The simple arrangement used here could easily be replaced by a more complex supply with 10–15 V rails for the MOSFET drivers, and isolated floating supplies for the control circuitry if found necessary.

The calculated hysteresis band turn on threshold was around 230 mV, which equals 700 mA with the 0.33 Ω sense resistors used. This allows a power of around 1.9 W into 8 Ω to be delivered by the linear amplifier before the buck converter begins assisting. The hysteresis band is approximately 120 mV or $\Delta I \approx 350$ mA.

The RL pole frequency of the inductor and the minimum load resistance determines the power bandwidth of the current dumping buck converter [3]. Very little audio power is required at high frequencies, and the transients can all be handled by the linear amplifier with little concern about power dissipation. Hence, a power bandwidth of 5 kHz into an 8 Ω load was chosen as a good compromise to reduce the ripple current for a given switching frequency. This leads to an inductor value of 220 μH.

Since all the ripple current is "absorbed" by the linear amplifier, this must also be kept reasonable to minimize power dissipation. In the conventional SMALA topology with the hysteresis band centred about zero current (Fig. 2), the linear amplifier must alternately source and sink the ripple current to cancel it. This leads to a constant power dissipation independent of output current of $V_{\mathrm{CC}} * \Delta I/2$ for a class A output stage, or $V_{\mathrm{CC}} * \Delta I/4$ for class B [3]. For this amplifier, that would be a modest $20 * 0.35/2 = 3.5$ W. This is however almost 20% of the amplifier's output rating, and may be quite significant in a higher power amplifier. It also means the linear amplifier is operating at high frequency around its cross-over point, which is most challenging from a distortion perspective.

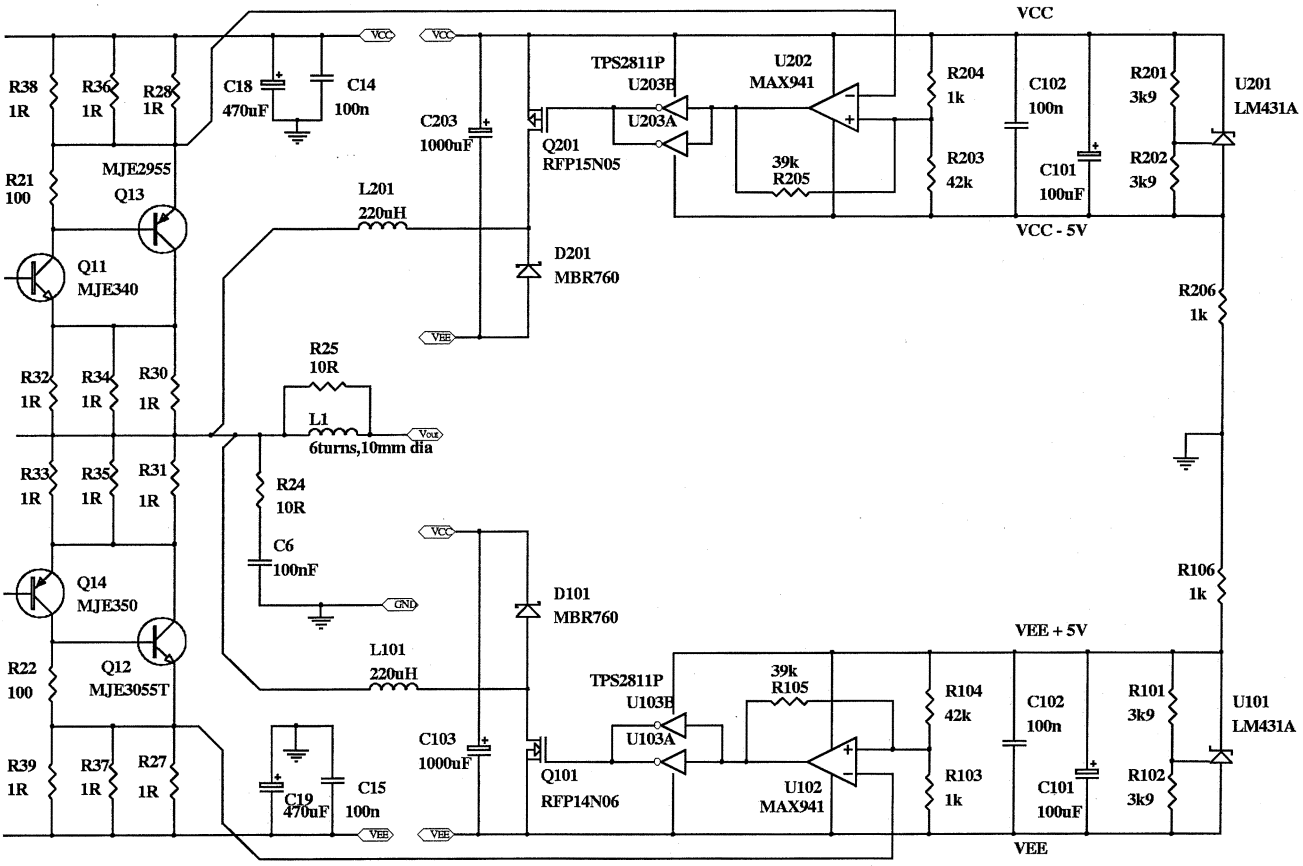

Fig. 7. Class-D buck converter circuit as implemented.

Because of the offset of the hysteresis bands of the switch-mode assistance, this class B linear amplifier is not faced with this challenge when cancelling the high frequency ripple current component. Instead this ripple current flow is either being cancelled at the summing point either entirely by the upper device as it sources current during the positive half cycle or by the lower device as it sinks current in the negative half cycle. This also reduces the power dissipation due to the ripple component, which partially compensates for the continuous current which must now also be sourced by the linear amplifier. In the limit, if the same hysteresis band is kept, with its lower threshold just above 0 (i.e., $I_{\rm on} = 0.36$ A, $I_{\rm off} = 0.01$ A), the power dissipation is equal to the class A case, $V_{\rm CC} * \Delta I/2 = 3.5$ W, but with the added advantage of pure linear operation to power levels of $I_{\rm on}^2 * R_L/2 = 0.5$ W here.

In this first implementation, a larger deadband has been chosen, with minimal compromise in power dissipation due to the low rated power output.

Like any hysteresis controller producing a varying output, the switching frequency will not be fixed. The maximum switching frequency occurs at the minimum output voltage (closest to zero), and the frequency goes to zero as the output voltage approaches the supply. The maximum switching frequency is [3], $f_{\rm sw,max} = V_{\rm CC}/(2L\Delta I) = 20\,{\rm V}/(2 * 220\,\mu{\rm H} * 0.35\,{\rm A}) = 130$ kHz.

The physical layout is contained on a double sided PCB similar in size to the class B amplifier (Fig. 9). The PCB was

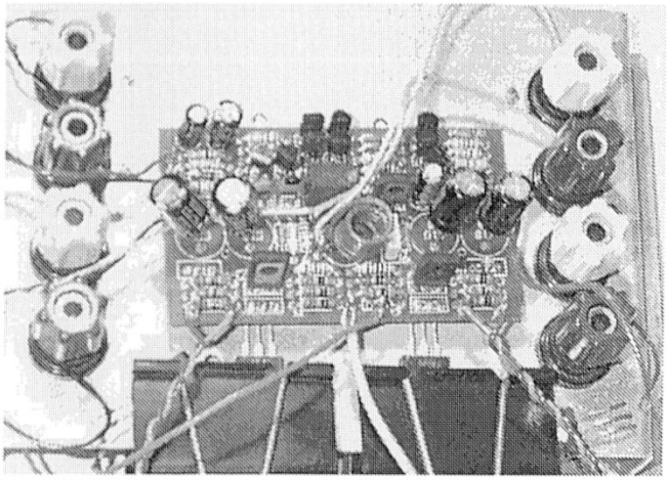

Fig. 8. Class-B linear amplifier PCB. The output BJT's are at bottom, under bulldog clips. Current sense leaves on twisted pairs from the bottom corners of PCB to buck converters (underside). The current assist returns on central wire.

placed on the reverse side of the metal chassis to the class B amplifier. TO-220 devices are used for the switching output devices, clamped in place on the plate chassis using the same fold-back spring clips holding the class B devices, and again insulated using thermally conductive pad material. This back to back sandwich layout with the metal chassis in between was hoped to reduce any noise coupled between the amplifiers, but allow for short interconnections.

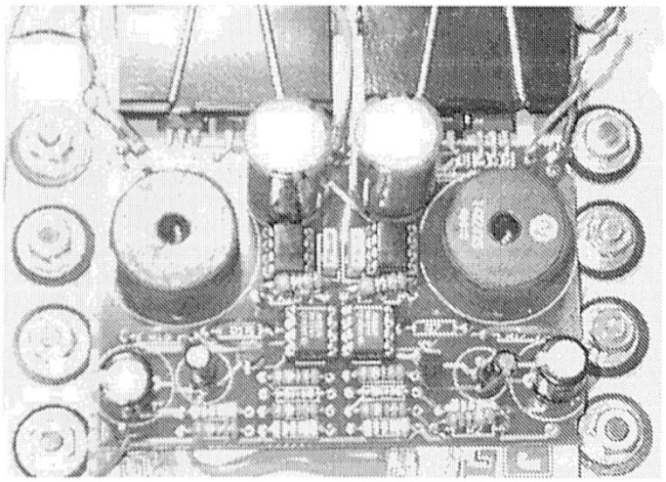

Fig. 9. Class-D buck converter circuit PCB, on the reverse side to the class-B PCB. The output MOSFETs and diodes are at top under bulldog clips.

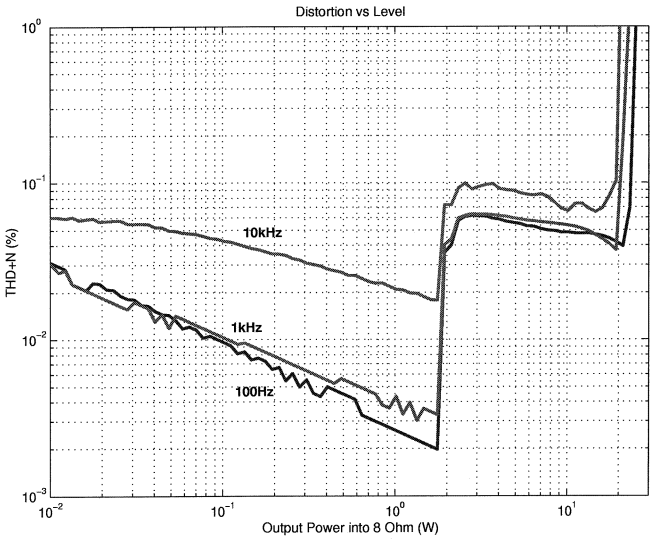

Fig. 10. Total harmonic distortion plus noise performance (THD+N, 22 Hz–80 kHz measurement bandwidth) in percent plotted against RMS output power at three frequencies: 100 Hz, 1 kHz, and 10 kHz.

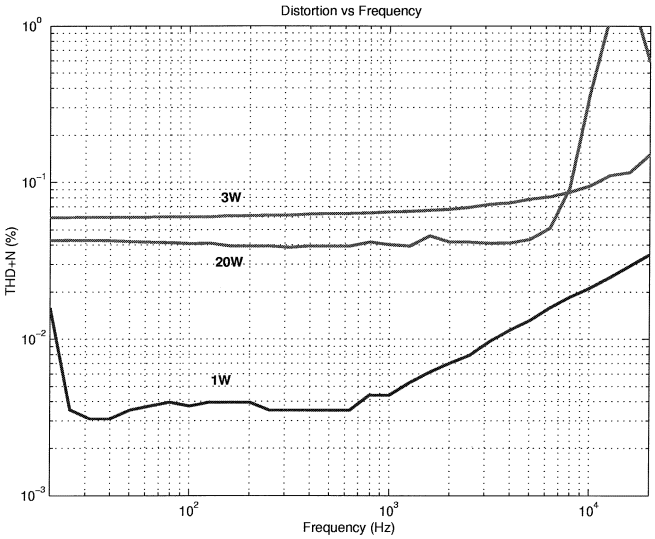

Fig. 11. Total harmonic distortion plus noise performance (THD+N, 22 Hz–80 kHz) in percent plotted against frequency for three RMS output power levels: 1 W (linear alone), 3 W (beginning of assistance), and 20 W (just prior to clipping).

III. Results

All measurements of the audio performance of the amplifier were gathered using an Audio Precision System One test set. The distortion measurements quoted are THD+N (total harmonic distortion plus noise) measured over a 22 Hz–80 kHz bandwidth. The 80 kHz upper frequency will include more noise, but is necessary to capture the harmonic distortion components of tones at the top of the audio spectrum. All measurements were taken with regulated ± 20 V supplies and an 8 Ω load.

A. Class B Linear Amplifier Performance

The linear class B amplifier had a measured closed loop bandwidth of approximately 300 kHz and a gain of 22 (27 dB). The measured residual noise figure (unweighted) was 87 dBV or 42 μV over the audio (22–22 kHz) bandwidth, to give a dynamic range of approximately 110 dB. The noise figure was unaffected by the presence of the buck converters as expected, since these are idle under no signal conditions.

The distortion performance of the class B amplifier alone was excellent, achieving the levels suggested possible by Self [7].

B. Overall SMALA Audio Performance

The distortion performance of the SMALA amplifier was also excellent, equalling the best linear amplifiers upto the point at which the buck converters began to assist (around 2 W). At this point distortion still stayed under 0.1% which would be perfectly acceptable for sound reinforcement applications.

Two distortion graphs are presented here, one vs. power for three fixed frequencies (Fig. 10), and one vs. frequency for three power levels (Fig. 11). The three fixed frequencies chosen are 100 Hz, 1 kHz, and 10 kHz. The three power levels chosen are 1 W, just before switchmode assistance begins, 3 W, just after assistance begins, and 20 W, just before clipping occurs. At frequencies beyond 6 kHz at 20 W, distortion rapidly rises due to the limited slew rate of the class D amplifier. This places a greater load on the class B amplifier, which then begins to clip at these higher frequencies. It is predicted that testing at a slightly lower power rating or with higher voltage rails would have produced a flat distortion response at full power.

The efficiency (Fig. 12) and power consumption/dissipation (Fig. 13) of the amplifier follows the expected theoretical class B efficiency and power dissipation up until the 2 W level when switchmode assistance begins. At this point, the total power dissipation for the switchmode assisted amplifier actually falls as power levels rise. This occurs because the linear amplifier passes a constant current set by the switchmode hysteresis controllers, but has less average voltage across the output devices and so decreasing power dissipation as output power levels rise. An efficient switchmode stage should always have a power dissipation which starts from near zero at low currents, and is lower than the linear amplifier even at full power.

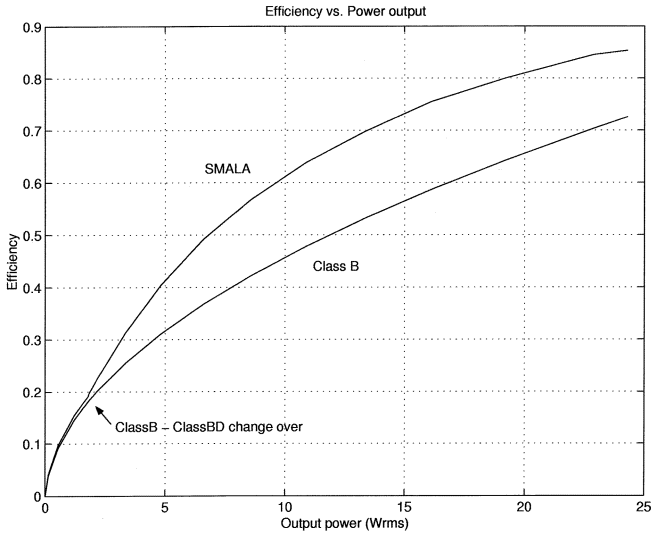

Fig. 12. Overall measured efficiency versus RMS output power of the SMALA showing the improvement compared to a conventional class-B linear amplifier (Measured with 20 V rails, 7.5 Ω load).

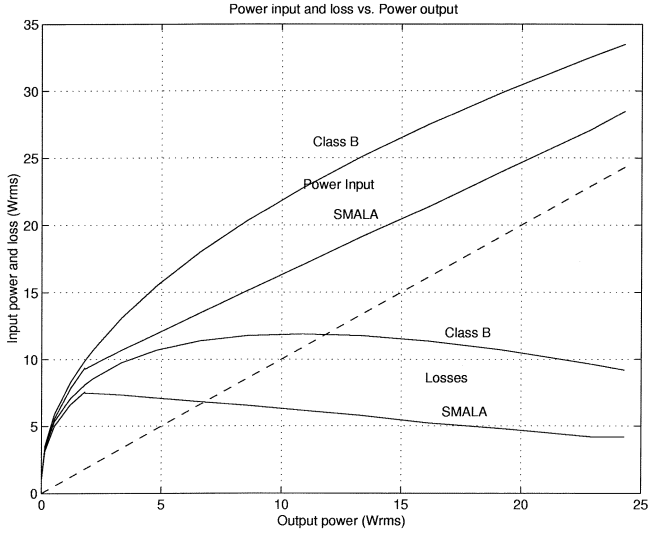

Fig. 13. Overall measured power consumption and power loss (dissipation) versus output power of the SMALA showing the improvement compared to a conventional class-B linear amplifier (Measured with 20 V rails, 7.5 Ω load).

An oscilloscope plot (Fig. 14) shows the switchmode stage output voltage measured across the upper MOSFET and the voltage drop across the upper sense resistor of the linear output stage, which is the input to the hysteresis controller. The power level is approximately 1.6 W, and the switchmode assistance has just begun at the crest of the output waveform as expected. The switching frequency seen is approximately 160 kHz. Any negative effects due to the ringing between the switchmode inductor and device capacitances observed at the end of the assistance cycle will be investigated in future research.

Spectral analysis of the amplifier output at various signal frequencies and output powers did not show any strong switching harmonic components. This is as expected due to the varying switch frequency of the hysteresis based control technique used. An example spectra of a 1 kHz full power output waveform (Fig. 15) shows any switching noise below 100 kHz to be more

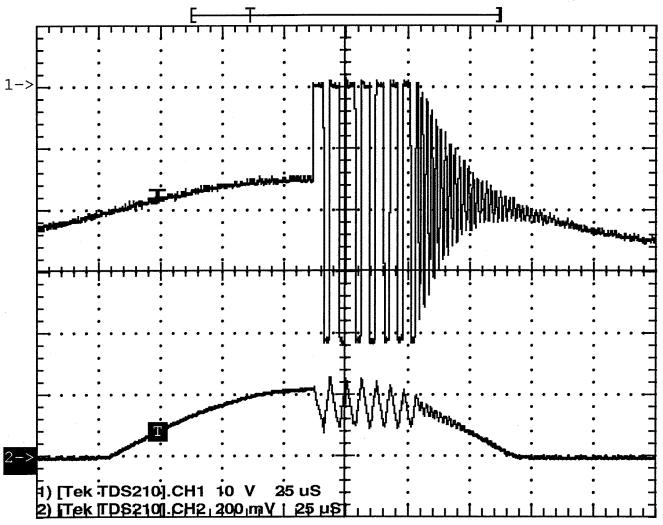

Fig. 14. Oscilloscope plot of the voltage across the upper buck converter MOSFET (10 V/div) and the voltage across the upper sense resistor which controls it via the hysteresis controller (200 mV/div). This shows the beginning of switchmode assistance at 1.6 W. (Time base is 25 μs/div.)

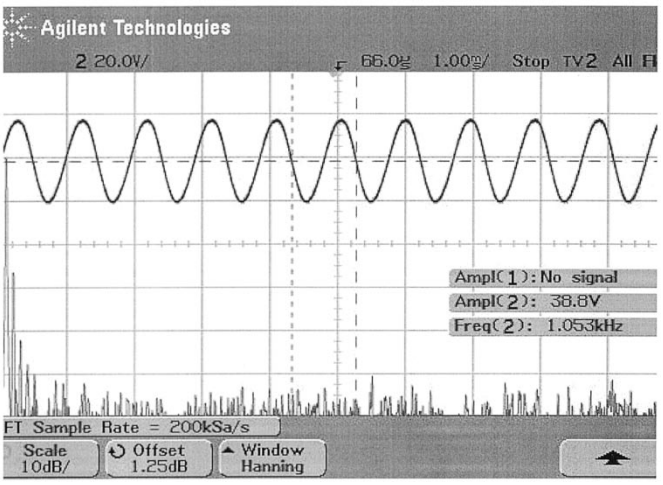

Fig. 15. Oscilloscope time domain and spectral plot of the amplifier output voltage at 1 kHz just prior to clipping. The spectrum scales are 10 kHz/div, and 10 dB/div. The FFT was performed using a Hanning window.

than 50 dB below the fundamental tone. The harmonic distortion evident in the 1 kHz test tone is actually a faithful reproduction of the lab signal generator's distortion.

IV. Conclusion

A new control strategy for the switchmode assisted linear amplifier topology is proposed and experimentally verified. Two separate buck converters assist each linear amplifier leg, using two separate hysteretic current controllers, one for positive excursions, and one for negative. A deadband around 0 V ensures only the linear amplifier operates at low power levels, to achieve excellent distortion and noise performance expected for audio applications. Efficiency is only slightly compromised compared to the original single bridge topology, and is still a large improvement on conventional linear amplifiers.

The next research goal is to implement this amplifier topology with high voltage rails of 80 V, to achieve 400 W output into

8 Ω. One key challenge at this higher voltage is creating the necessary wide gain-bandwidth linear amplifier with high voltage devices. The other research goal is to implement a multilevel switchmode assistance topology with a carrier based current controller.

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